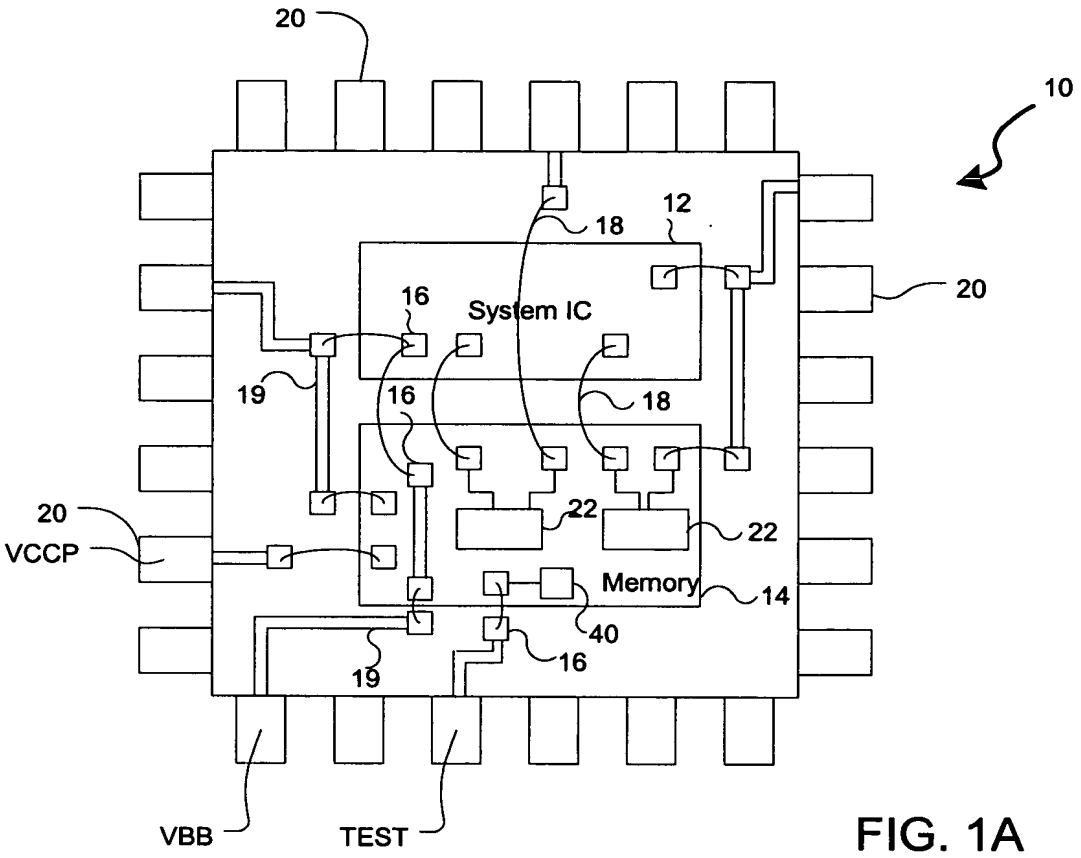
20
10
12
18
20
16
System IC
19
16
18
20
22
22
VCCP
Memory
14
40
16
19
VBB
TEST

FIG. 1A

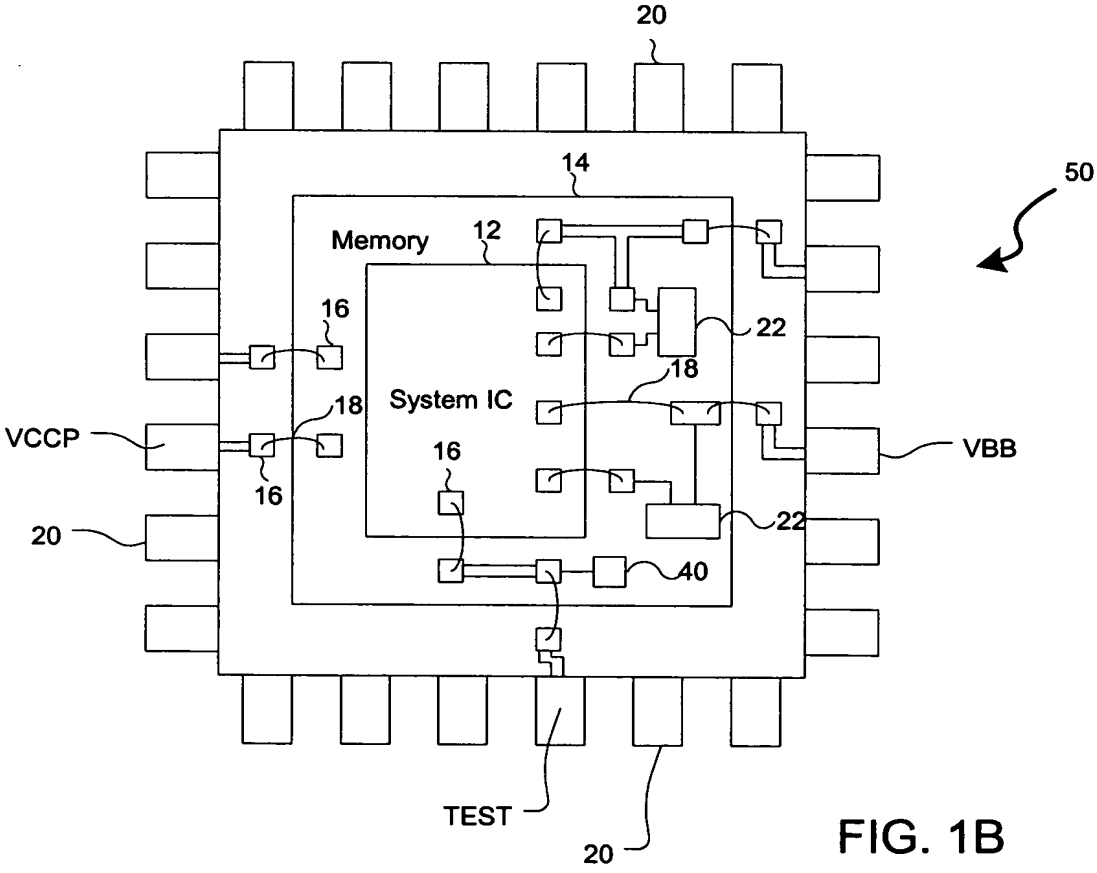
20
14
50
Memory
12
16
22
18
18
System IC
VCCP
VBB
16
16
20
22
40
TEST
20

FIG. 1B

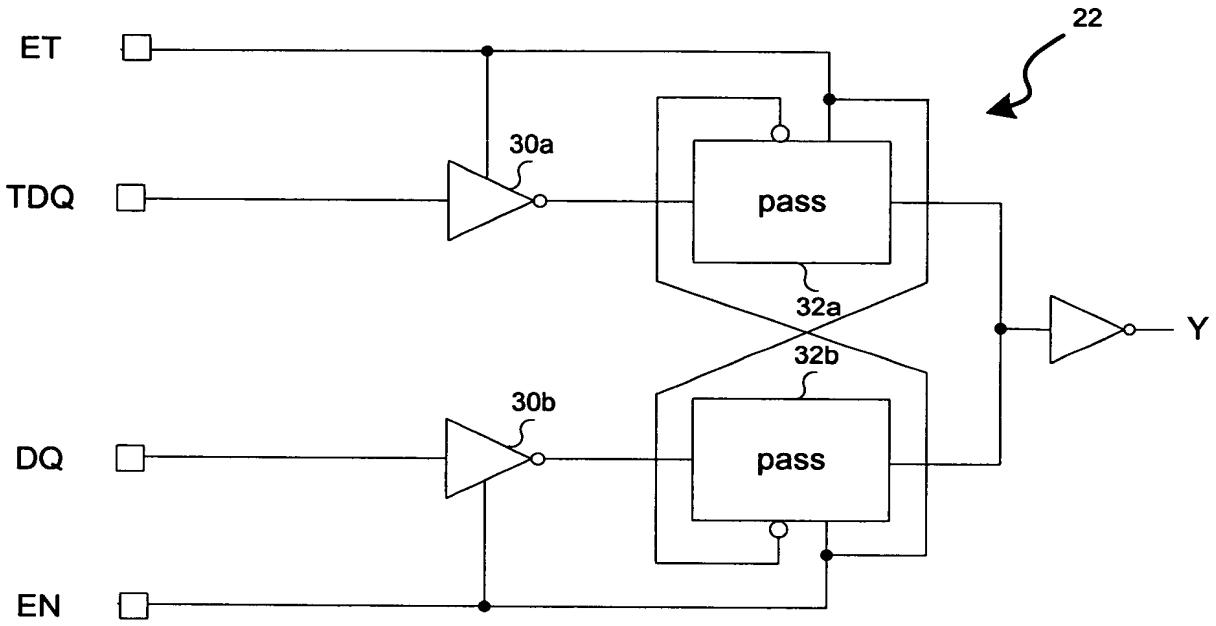
22
ET
TDQ
30a
pass
32a
32b
Y
30b
DQ
pass
EN

FIG. 2A

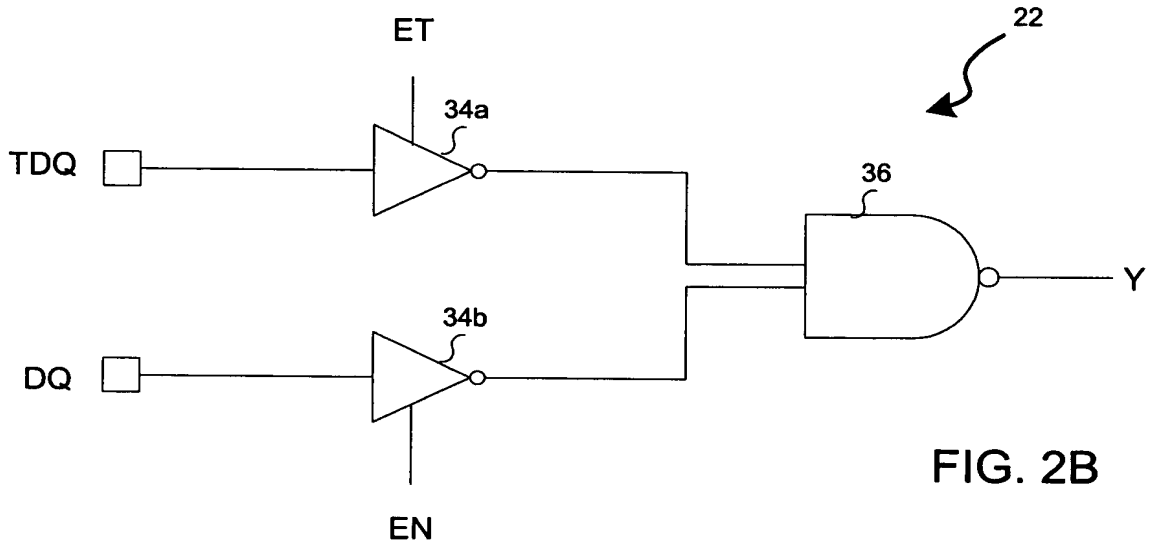
ET
22
34a
TDQ
36
Y
34b
DQ
EN

FIG. 2B

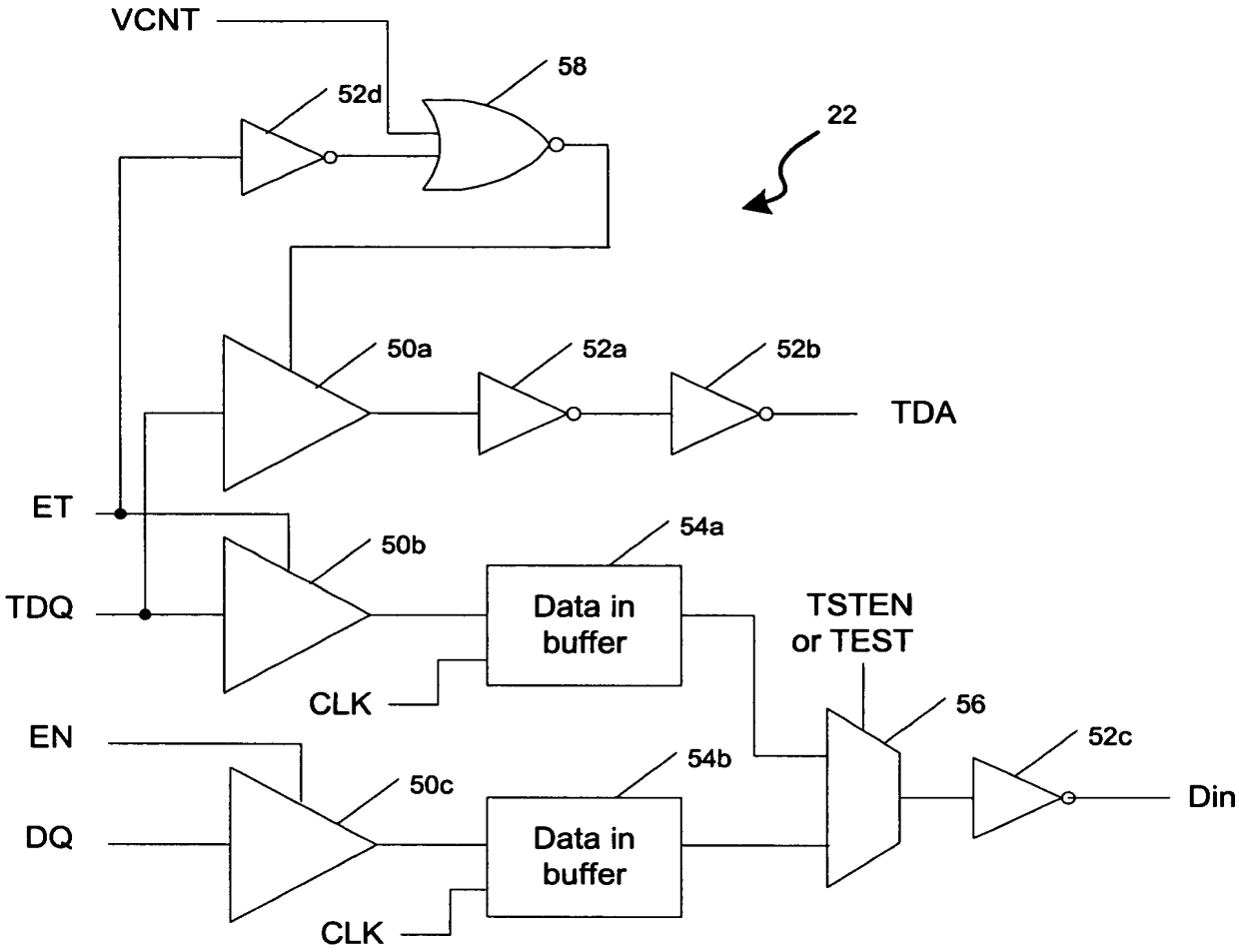
VCNT
58
52d
22
50a
52a
52b
TDA
ET
50b
54a
TDQ
Data in buffer
TSTEN or TEST
CLK
56
EN
52c
54b
50c
Din
DQ
Data in buffer
CLK

FIG. 2C

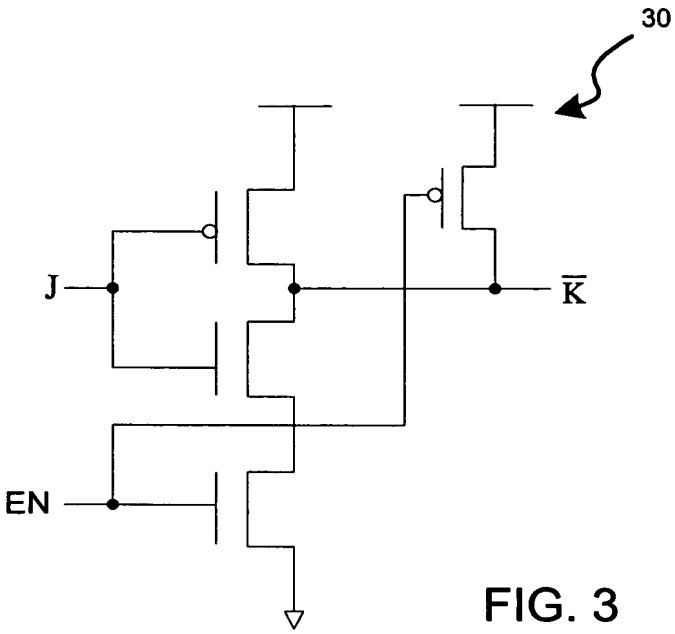

FIG. 3

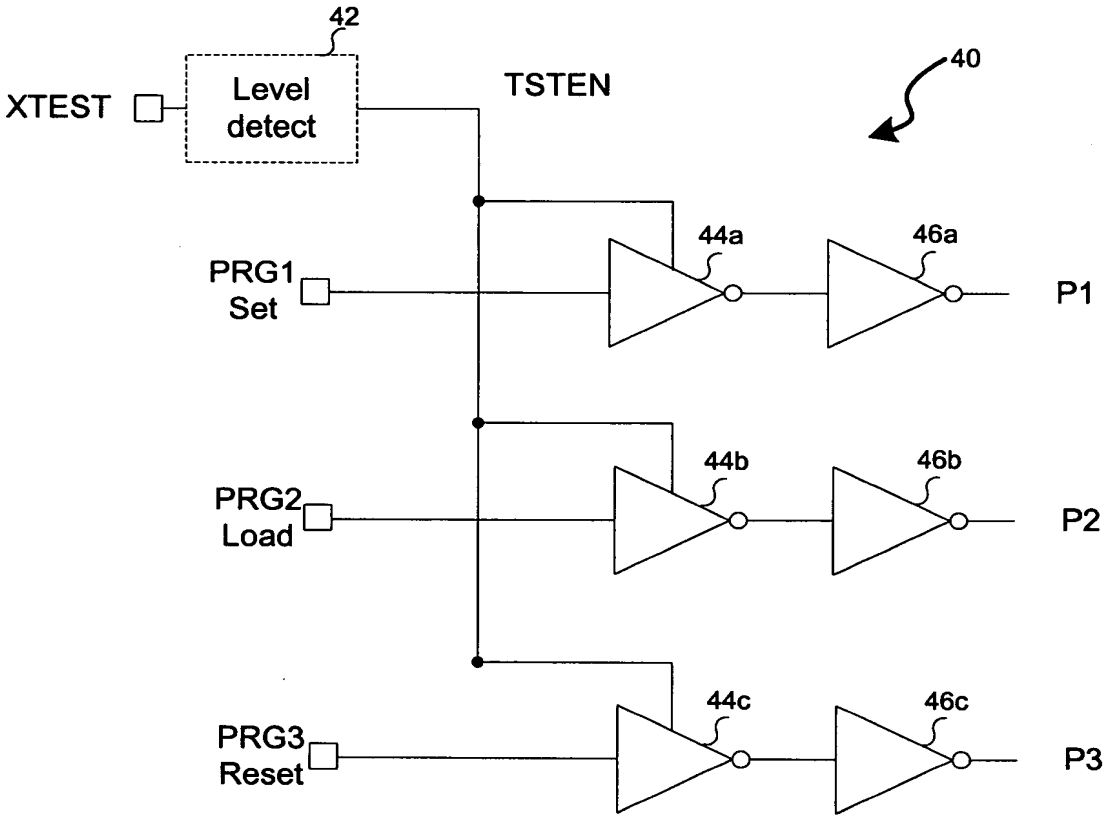
42
XTEST
Level detect
TSTEN
40
44a
46a
PRG1 Set
P1
44b
46b
PRG2 Load
P2
44c
46c
PRG3 Reset
P3

FIG. 4

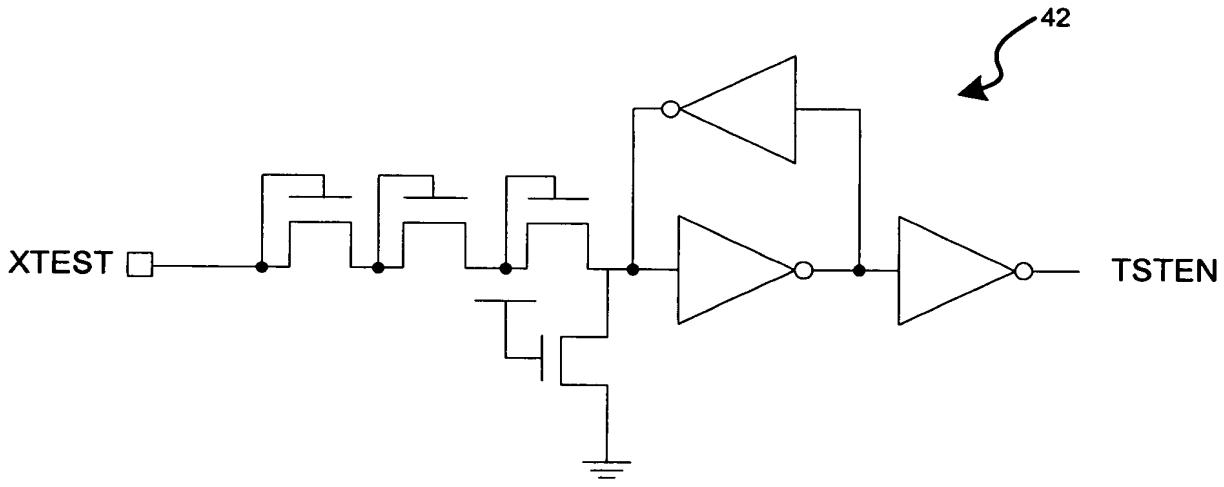
42
XTEST
TSTEN

FIG. 5

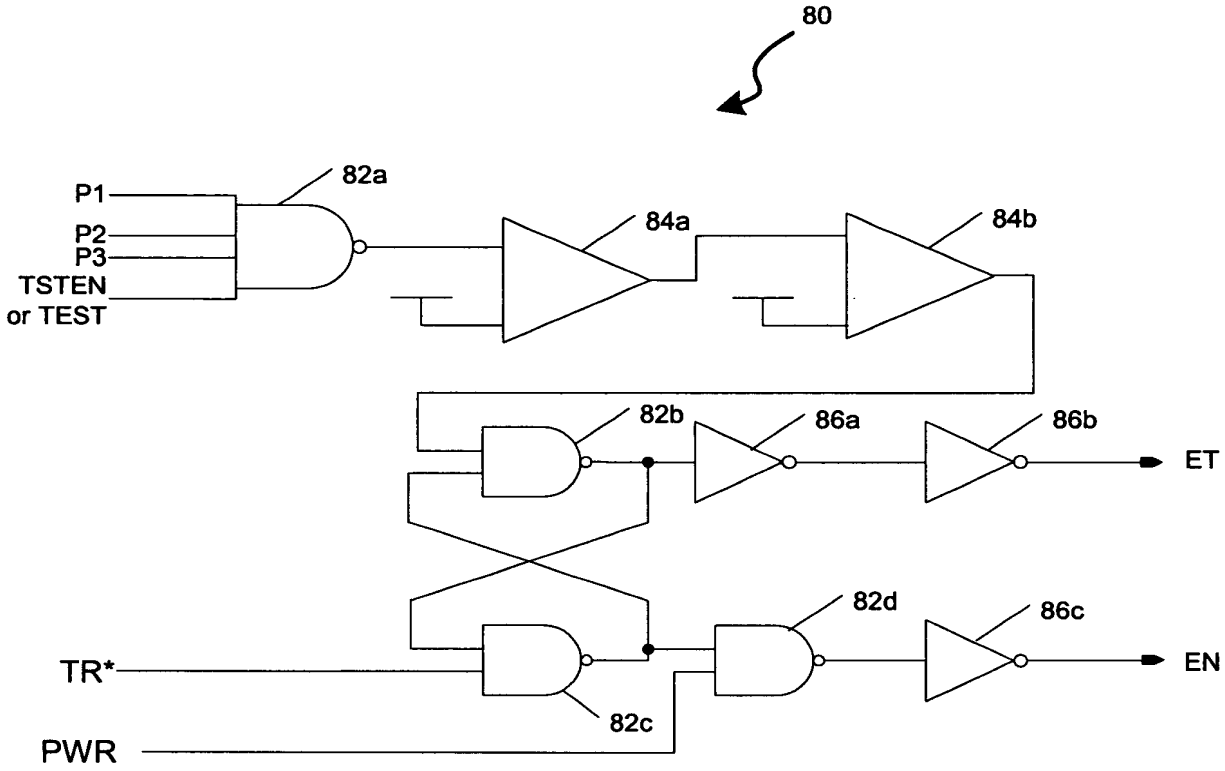
80
82a
P1
P2
P3
TSTEN
or TEST
84a
84b
82b
86a
86b
ET
82d
86c
EN
TR*
82c
PWR

FIG. 6

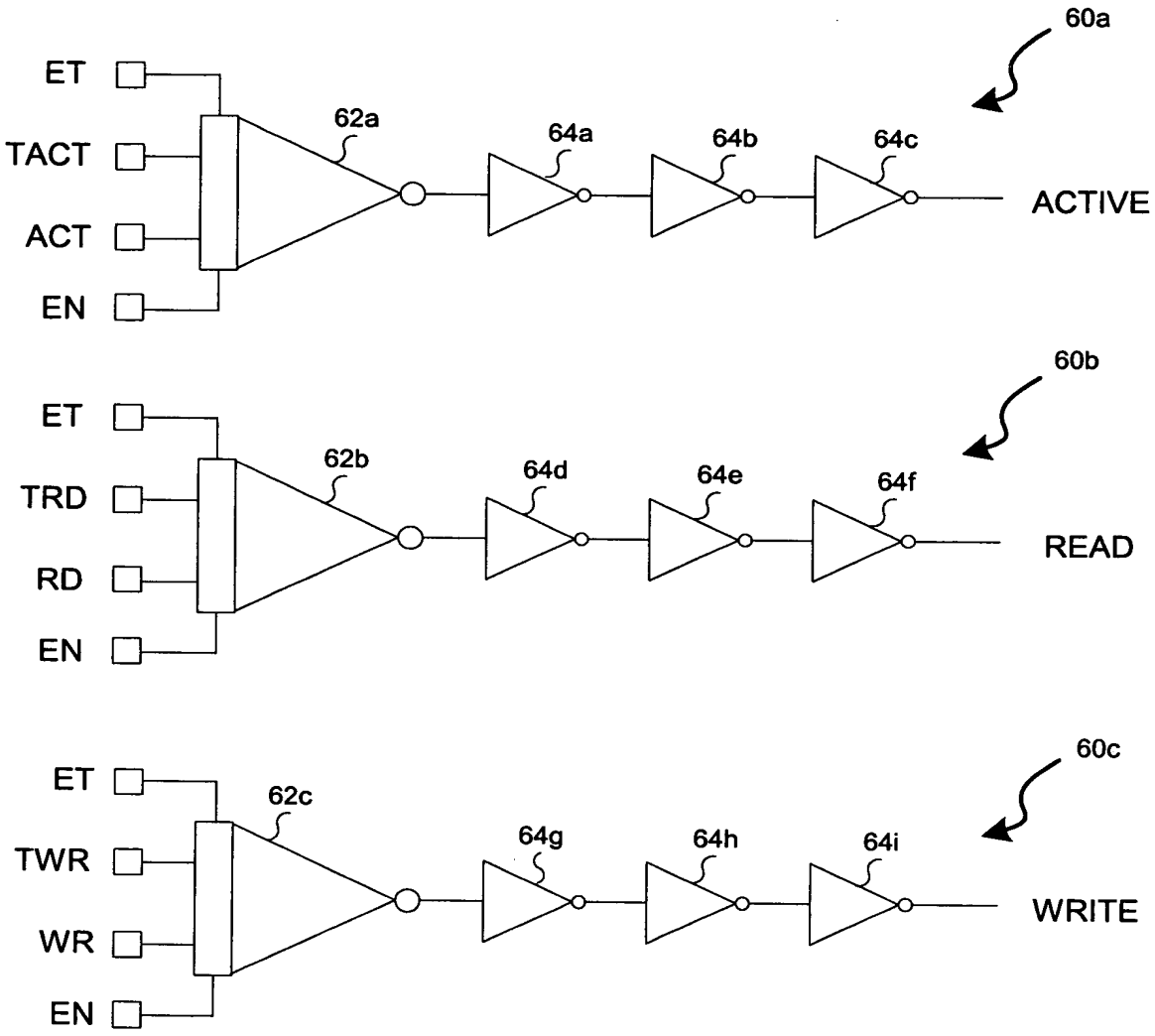
60a
ET
TACT
ACT
EN
62a
64a
64b
64c
ACTIVE
60b
ET
TRD
RD
EN
62b
64d
64e
64f
READ
60c
ET
TWR
WR
EN
62c
64g
64h
64i
WRITE

FIG. 7

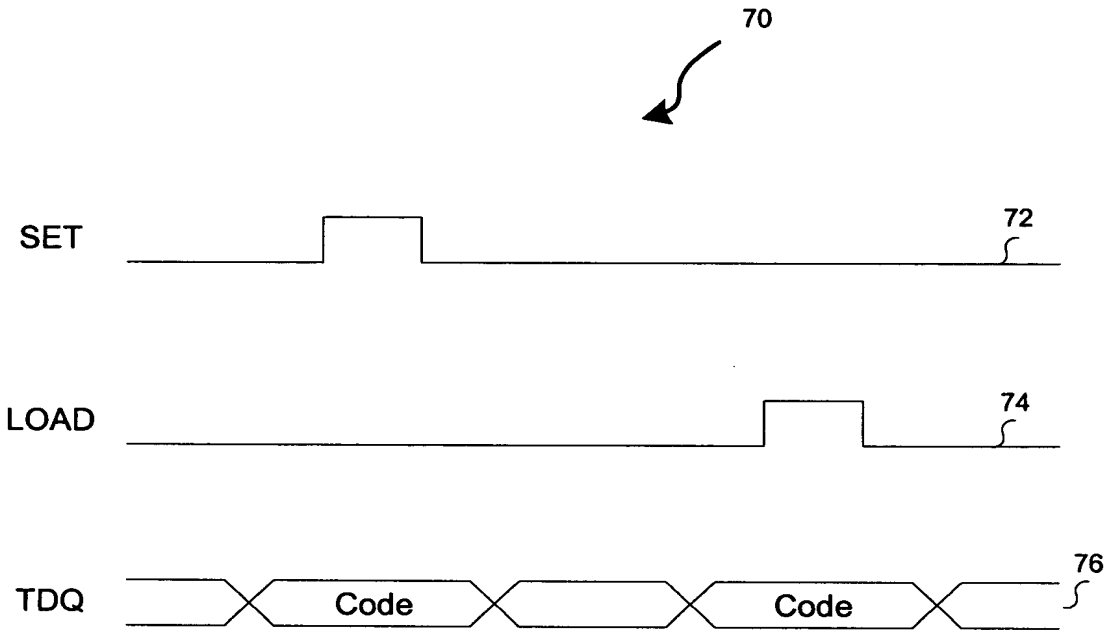

FIG. 8

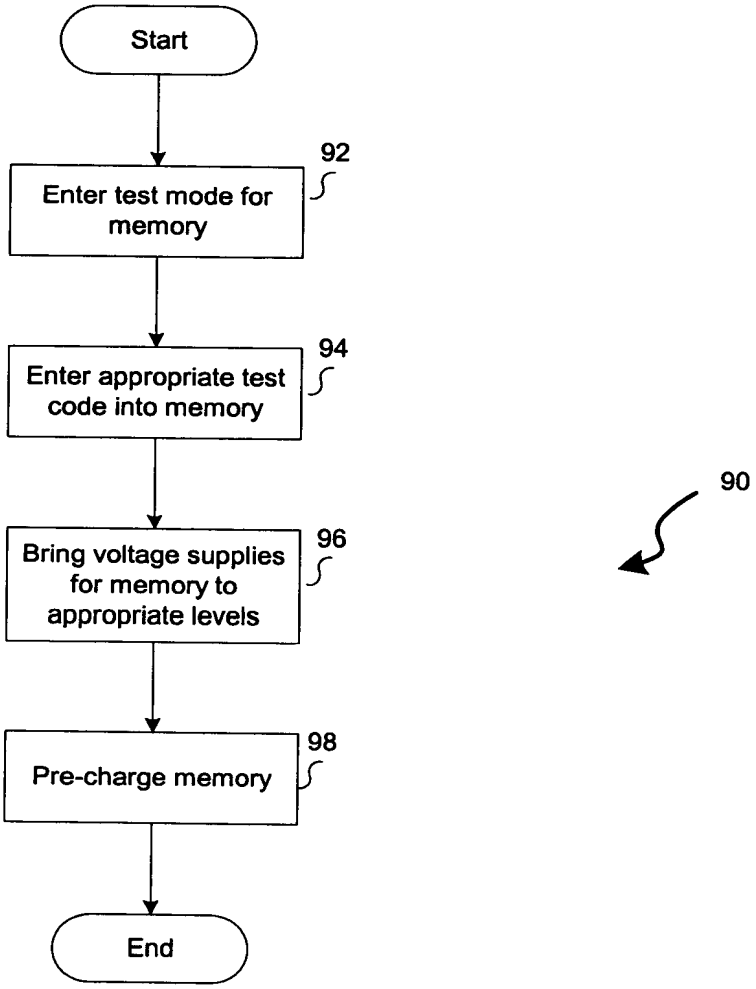
Start
92
Enter test mode for memory
94
Enter appropriate test code into memory
96
Bring voltage supplies for memory to appropriate levels
98
Pre-charge memory
End
90

FIG. 9

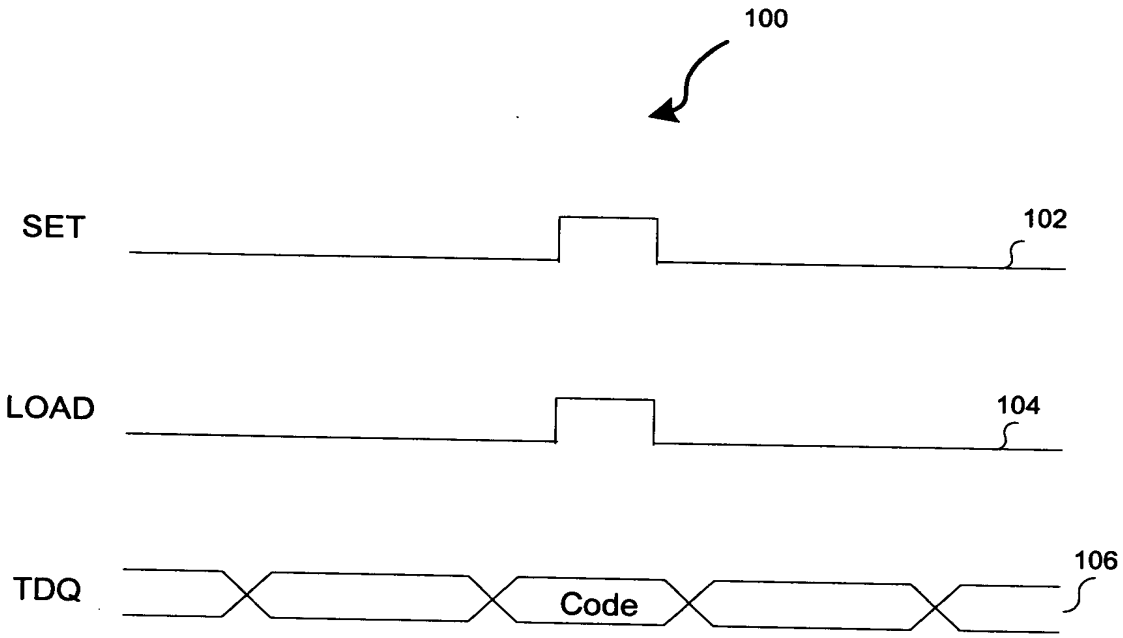

FIG. 10